AK

Notice of Allowability	Application No.	Applicant(s)	
	10/811,830	KAWASHIMA ET AL.	
	Examiner	Art Unit	
	Victor V Yevsikov	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *paper, filed 03/30/04*.

2. ☒ The allowed claim(s) is/are *21-45*.

3. ☒ The drawings filed on *20 March 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 032004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Claim 21, line 14,

"region is formed is formed" should read as -- region is formed--.

Appropriate correction is required.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Melvin Kraus (Reg. No. 22,466) on September 23, 2005.

Allowable Subject Matter

Claims 21-45 are allowed.

The following is an examiner's statement of reasons for allowance:

Prior art does not teach a semiconductor device having a nonvolatile memory cell wherein:

a second semiconductor region of a second conduction type opposite to the first conduction type formed in the semiconductor substrate below the second gate electrode, and wherein a main surface of the semiconductor substrate in which the second semiconductor region is formed is formed so as to be lower than a main surface of the semiconductor substrate in which the first semiconductor region is formed; and

an end portion of the second semiconductor region at the side of the second field effect transistor coincides with a position of an end portion of the second gate electrode at the first field effect transistor side and the gate insulating film or extends so as to be partly below a region of the second gate electrode and the gate insulating film; and

a position of a side surface at an end in a width direction of the charge storage layer coincides with a position of a side surface at an end in a width direction of the gate electrode or is apart from the side surface at an end in the width direction of the gate electrode toward a center of the gate electrode; and

the charge storage layer is formed so that its whole region in plan view is included in a whole region of the gate electrode in plan view; and

the n-type gate electrode has a first region near the charge storage layer and a second region as another region, and concentration of n-type impurity in the first region is lower than that of the n-type impurity in the second region; and

concentration of n-type impurity in the n-type gate electrode is lower than that of the n-type impurity in a gate electrode of an n type in another field effect transistor provided over the semiconductor substrate; and

electrons in the charge storage layer are extracted to the gate electrode side and positive holes in the gate electrode are injected to the charge storage layer side and promoted to recombine with the electrons, thereby erasing data; and

concentration of n-type impurity in said n-type gate electrode is $1x10^{18}$/cm3 to $2x10^{20}$/cm3; and

concentration of n-type impurity in the n-type gate electrode is $8x10^{19}$/cm3 to $1.5x10^{20}$/cm3; and

electrons in the charge storage layer are extracted to the gate electrode side, thereby erasing data, and the gate electrode is of a p type; and

the lowest write level is higher than an initial threshold voltage of the nonvolatile memory cell.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor Yevsikov whose telephone number is (571) 272-1910. The examiner can normally be reached on Monday –Thursdays 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or processing is assigned is (703) 873-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information

about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

V. Yevsikov

Victor Yevsikov
Examiner
Art Unit 2825

December 9, 2005

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
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